ASIC Design and Test Methodologies
EE5375 / EE4395, Fall 2013, UTEP / NMSU
Department of Electrical and Computer Engineering

Basic Information

<table>
<thead>
<tr>
<th>Instructors</th>
<th>Eric MacDonald</th>
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<tbody>
<tr>
<td>Office</td>
<td>A310</td>
</tr>
<tr>
<td>Phone</td>
<td>747-6959</td>
</tr>
<tr>
<td>EMAIL</td>
<td><a href="mailto:emac@utep.edu">emac@utep.edu</a></td>
</tr>
<tr>
<td>Office hours</td>
<td>10:00am – 11:30am M – F</td>
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<tr>
<td>TAs</td>
<td>None supported</td>
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| Course Description | Theory, principles and techniques of fault modeling, simulation, testing and fault-tolerant design of digital logic circuits. Verilog hardware description language will be discussed and a series of labs will focus on the design, simulation, synthesis, timing, and implementation of an industry-styled ASIC. |
| Text            | None required. One recommended: Verilog HDL: A guide to Digital Design and Synthesis by Samir Palnitkar Course note pdfs to be emailed 24 hours prior to class |

| FPGA Board      | Basys2 boards will be used by teams of two in this class. $50. |
| Optional Software | none – final project and some home works will require using Cadence and Synopsys software on Unix workstations. Veriwell, Icurus and gtkwave are a free Verilog simulator / waveform viewer that runs on Linux, Cygwin or Mac – see webpage. |
| Prerequisites   | Undergrad logic design. Lab will require Verilog HDL but not as a prereq |
| Web page        | http://www.ece.utep.edu/courses/web5375 |

Grading EE5375

<table>
<thead>
<tr>
<th>Element</th>
<th>Weight</th>
<th>Comment</th>
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<tbody>
<tr>
<td>Three Midterms</td>
<td>10%</td>
<td>Open lecture notes only.</td>
</tr>
<tr>
<td>Final Exam</td>
<td>20%</td>
<td>Open lecture notes only - comprehensive</td>
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<tr>
<td>Home works</td>
<td>10%</td>
<td>Can be worked as teams, each student should turn in own copy</td>
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<tr>
<td>Labs</td>
<td>40%</td>
<td>Final project will be 20%, other labs 20%</td>
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### General Policies

I respond to all email within 24 hours of receiving the email. Consider all email to me as lost if I don’t respond within 24 hours. Use alternative method of contacting me in this case.

Homework and labs will not be accepted more than one week late (see exceptions below). If you miss class, contact the professor or a classmate to find out what work was assigned or if any important announcements were made.

The only exceptions for accepting late assignments include a medical emergency requiring hospitalization, jury duty, attendance of a funeral of an immediate member of your family, or official UTEP business. **Documentary proof of any of the above must be provided before or immediately after the fact.**

American Disabilities Act: If you feel you may have a disability that requires accommodations, contact the Disabled Student Services Office at 747-5148 or go to room 106E of the Union.

The final project must be completed individually or in teams of two. Discussion of ideas is encouraged but any code that is obviously copied will be submitted to the Dean of Students for plagiarism.

**Academic Dishonesty – See course website for details.**

**Grading Scale**

<table>
<thead>
<tr>
<th>Percentage</th>
<th>Grade</th>
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<tbody>
<tr>
<td>100% to 90%</td>
<td>A</td>
</tr>
<tr>
<td>89% to 80%</td>
<td>B</td>
</tr>
<tr>
<td>79% to 70%</td>
<td>C</td>
</tr>
<tr>
<td>69% to 60%</td>
<td>D</td>
</tr>
<tr>
<td>&lt;60%</td>
<td>F</td>
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No curve will be used. However, 5 total points of extra credit will be offered to all students throughout the semester.

**Remote Students:** This is not an on-line course. Some lectures and course materials may be made available through the internet to help remote students, however provision of these materials is not guaranteed and the corresponding quality may be insufficient for learning the course material. Remote students will be held to the same deadline and standards as to non-remote students. Non-remote students will not be given access to recorded lectures and are expected to attend class.

Term projects will be submitted to MOSIS for fabrication in ON 0.5u CMOS technology available the following April. Possible to get individual studies class on the evaluation and characterization of the chip.

No exam make-ups will be allowed. The final exam will replace the lowest grade of the three mid-terms however for all students. If the final project is completed on time and if the exam grade is acceptable to the student prior to the exam, the three mid-terms can replace the final exam.