Lesson 10: Moore Machine

Sequential vs Concurrent Statements
- VHDL is inherently a concurrent language
  - All VHDL processes execute concurrently
  - Concurrent signal assignment statements are actually one-line processes
- VHDL statements execute sequentially within a process
- Concurrent processes with sequential execution within a process offers maximum flexibility
  - Supports various levels of abstraction
  - Supports modeling of concurrent and sequential events as observed in real systems

Sequential Statements
- Statements inside a process execute sequentially

Attributes
- Attributes provide information about certain items in VHDL
  - E.g. types, subtypes, procedures, functions, signals, variables, constants, entities, architectures, configurations, packages, components
- VHDL has several predefined, e.g.:
  - X'EVENT -- TRUE when there is an event on signal X
  - X'LAST_VALUE -- returns the previous value of signal X
  - Y'HIGH -- returns the highest value in the range of Y
  - X'STABLE(t) -- TRUE when no event has occurred on signal X in the past 't' time

Sequential Circuits
- Process Statement
  - process(clk)
  - process (sensitivity list)
  - Begin
  - If (clk='1')
    - Sequential statements
  - end process;

D Flip-Flop
- process (CLK)
  - begin
    - if clr='1'
      - Q<=0;
    - else if CLK'event and CLK = '1'
      - then Q<=D;
    - end if;
  - end Process;
How to find the rising edge of clock?

if RST='1' then
    ----
elsif CLK'event and CLK = '1' then
    case current is
        ..
        ..
    end case;
end if;

Types of State Machines

- Moore State Machines
  - Inputs and current state determine next state
  - Only current state determines output
  - For counters, current state is output - thus Moore

- Mealy State Machines
  - Inputs and current state determine next state
  - Inputs and current state determine output
  - Design is generally smaller than Moore
  - Input glitches can translate directly to outputs

Moore State Machines

Moore State Machine Example

State Graph and Table for Moore

Output value is tied to current state and is therefore included in bubble. Inputs determine next state.
Simple Mealy example – serial adder

State Graph for Mealy example

General Example of State Tables for Mealy

Sequence Detector Example

- Very common interview question for design jobs
- One input and one output
  - Input represents sequential list of 1’s and 0’s
  - Output asserts if specific sequence is detected
- In this example, the prescribed sequence is 101

\[ X = 0 \ 0 \ 1 \ 1 \ 0 \ 1 \ 1 \ 0 \ 0 \ 1 \ 0 \ 1 \ 0 \ 1 \ 0 \ 0 \]
\[ Z = 0 \ 0 \ 0 \ 1 \ 0 \ 0 \ 0 \ 0 \ 1 \ 0 \ 1 \ 0 \ 0 \]

State graph for Moore detector

State Table for Moore sequence detector
Lab 8 – Sequence Detector

- Input Ports – Clk, input (X), Reset
- Output Ports – output (Z), State

architecture behave of SEQDET is

begin
process (CLK, rst)
if reset = '1'

case state is
when S0 =>
if (x = '0') then state <= ….
else ….
end if;
when others => null;
end case;
end if;
else (clk'event and clk=1)
……
end process;
end ….