EE 5390 Final Project Report:

Design of a
Narrowband Low-Noise Amplifier and Mixer

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I. ABSTRACT

The focus of this project is the design of a narrowband 0.5 µm CMOS low-noise amplifier and mixer operating in the 900 MHz frequency range using Agilent ADS EDA tool. The LNA and mixer were designed to meet the specifications provided by Dr. Yao.

II. OBJECTIVES

The project entails the design a 0.5 µm CMOS circuit that satisfies the functional requirement of a Low Noise Amplifier (LNA) and mixer in the 940 - 980 MHz range and to simulate this circuit using the ADS software.

The following are the objectives of this design project:

• The design of the circuit for the project
• Extensive circuit simulation with Agilent ADS
• A typewritten technical report

III. LNA AND MIXER OVERVIEW

The basic structure of a RF front-end is depicted below:

![RF Front-end Diagram]

*Figure 1. RF Front-end*

The LNA is usually the first stage of any receiver. This stage provides enough gain to overcome noise of subsequent stages [1]. It should offer as little noise as possible to large signals and at the same time provide good linearity. A narrowband cascode design topology was used in this project because of its good frequency performance [2]. An LNA design presents a considerable challenge because of its simultaneous requirement for high gain, low noise figure, good input and output matching and unconditional stability at the lowest possible current draw from the amplifier. Although
gain, noise figure, stability, linearity and input and output match are all equally important, they are interdependent and do not always work in each other’s favor [3].

In a radio frequency front end the incoming signal at the radio frequency (RF) is converted to the intermediate frequency by mixing with the local oscillator (LO) signal. The mixer inputs are RF and LO signals and the output is the IF signal. Typically many RF signals exist but only one is desired. This means that one of the main concerns in a mixer is linearity of the RF input to prevent inter-modulations between various input signals. Other issues of importance are frequency response, power dissipation and noise.

**IV. LNA DESIGN METHODOLOGY**

The design of the LNA circuit was a procedural process whereby different tasks were carried out in a step-by-step basis so as to organize the design process in a logical manner starting with the specifications provided, followed by the choice of circuit topology, design and finally simulation to see that the circuit meet the requirements.

The specifications listed in Table 1 are the given specifications for the LNA and mixer. These specifications were the basis upon which the circuit was deigned:

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency range</td>
<td>940 MHz to 980 MHz</td>
</tr>
<tr>
<td>Input Impedance Zin</td>
<td></td>
</tr>
<tr>
<td>Voltage Gain Av</td>
<td>&gt;20 dB</td>
</tr>
<tr>
<td>Noise Figure</td>
<td>(50 $\Omega$) &lt; 3 dB</td>
</tr>
<tr>
<td>$P_{1\text{dB}}$</td>
<td>&gt; -20 dBm</td>
</tr>
<tr>
<td>IIP$_3$</td>
<td>&gt;-10 dBm</td>
</tr>
<tr>
<td>Total Current</td>
<td>&lt; 5 mA</td>
</tr>
</tbody>
</table>

*Table 1: LNA Specifications*

For this project, 0.5 μm CMOS technology was chosen which means that all the transistors used in the circuit had a length of 0.5 μm. In addition, NMOS devices were
used instead of PMOS transistors because their high transconductance allows for an improved $f_t$ [5].

The circuit topology used for the LNA is directly related to its role as the first module of a receiver. Its main functions are to amplify and maintain the linearity of the receiver and to minimize the amount of noise added to the system. A single-ended cascode topology using a Common-Source amplifier was adopted.

The Common-Source (CS) amplifier acts as the driver of the LNA. This topology was chosen because it provides a high voltage gain, which is an important requirement of the design. In addition, the CS amplifier provides good linearity. However, the biggest disadvantage of the CS amplifier is its limited high-frequency response, which is due to the presence of $C_{gd}$, an internal capacitance that is connected between the gate and drain. [6].

![Fig 2: LNA circuit used for AC simulation](image_url)
In order to improve the high frequency behavior of the LNA, the cascode configuration was employed. The cascoding transistor is used to reduce the interaction of the tuned output with the tuned input and also to reduce the effect of the amplifying transistor’s $C_{gd}$ [3].

The current mirror was used to produce a stable reference current that can be used to produce proportional DC currents for biasing other transistors in the circuit. In this case, two CMOS transistors were used to drive the CS amplifier and the cascode transistor. The biasing transistors are fed with a reference current, which is fixed using a DC source. Since the transistors were biased such that $V_{gs} > V_t$ and $V_{ds} > V_{gs} - V_t$ for the CS transistor, the output drain current of the CS amplifier is a function of the reference current, as well as the width and length of both transistors [3].
Quantitative Analysis:

\[
L_2 = \frac{50\Omega}{2\pi \times 4GHz}
\]

\[
NF = 1 + \frac{2}{3} \frac{1}{1 + \frac{L_1}{L_2}} < 3
\]

\[
\omega_c (L_1 + L_2) = \frac{1}{\omega_c C_{gs}}
\]

\[
W = \frac{C}{2} \frac{2}{3} C_{ox} L
\]

\[
gm = \sqrt{2k\left(\frac{W}{L}\right)_1 I_{D1}}
\]

V. MIXER DESIGN METHODOLOGY

The Mixer Design specifications are as follows:

<table>
<thead>
<tr>
<th>RF input:</th>
<th>( V_{RF} = 0.001 \sin(2\pi f_{RF}t) ) V where ( f_{RF} = 960 ) MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>LO (positive node):</td>
<td>( V_{LO+} = 2 + 0.2 \sin (2\pi f_{LO}t) ) V where ( f_{LO} = 950 ) MHz</td>
</tr>
<tr>
<td>LO (negative node):</td>
<td>( V_{LO-} = 2 - 0.2 \sin (2\pi f_{LO}t) ) V where ( f_{LO} = 950 ) MHz</td>
</tr>
<tr>
<td>IF output:</td>
<td>( V_{IF} )</td>
</tr>
</tbody>
</table>

*Table 2: Mixer specifications*

In this design, \( V_{LO} \) is chosen such that the transistors alternately switch all of the tail current from one side to the other at the LO frequency. The tail current is therefore effectively multiplied by a square wave whose frequency is that of the local oscillator:

\[
I_{out}(t) = \text{sgn}[\cos(\omega_{LO}t)]\{I_{BIAS} + I_{RF}\cos(\omega_{RF}t)\} \ [6].
\]

Because of the presence of the LO in the output spectrum, the mixer used in this design project is known as a single-balanced mixer.

A linearized transconductance is incorporated. The value of the bias voltage establishes the bias current of the transistor. The values of the biasing resistors are chosen
to be large enough not to load down the gate circuit (and also to reduce its noise contribution [6]. The RF signal is applied to the gate through a DC blocking capacitor.

Fig 4: Mixer circuit schematic

VI. LNA SIMULATION RESULTS

The different types of analysis that were performed on the LNA are AC, Noise and scattering-parameter (s-parameter). These analyses were done to determine the total current, voltage gain, input impedance and noise figure of the LNA. The results are summarized in Table 3.

<table>
<thead>
<tr>
<th></th>
<th>Theoretical</th>
<th>Simulation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total Current</td>
<td>5 mA</td>
<td>6.2 mA</td>
</tr>
<tr>
<td>Voltage Gain</td>
<td>20 dB</td>
<td>27 dB</td>
</tr>
<tr>
<td>Input Impedance</td>
<td>50 Ω</td>
<td>48 Ω</td>
</tr>
<tr>
<td>Noise Figure</td>
<td>&lt; 3 dB</td>
<td>16 dB</td>
</tr>
</tbody>
</table>

Table 3: LNA Simulation results
Fig 5: AC gain of design circuit LNA

Fig 6: Clockwise from top left: Input impedance, s-parameter (1,1) and noise figures
VII. MIXER SIMULATION RESULTS

After successful simulation of the mixer circuit, a Harmonic Balance simulation was carried out and the output plotted. The RF input was at 950 MHz and the local oscillator frequencies were 940 MHz for both the positive and negative nodes.

The output at frequency = 10 MHz was seen to be 0.002. With an input voltage of 0.001 V, the gain is 0.002/0.001 = 2. In decibels, the mixer conversion gain is

\[ 20 \times \log (2) = 6.02 \text{ dB} \]

which is a very good result.

The following observations were made:

- The amplitude of the LO leakage output was observed to be 0.8 V
- The DC offset at the IF output was 44 µV
- The amplitude of the LO leakage at the RF input was 6 mV

Fig 7: Mixer output showing output voltages at different frequencies
VIII. CONCLUSION

A CMOS low noise amplifier operating at a supply voltage of 1.4 V and a center frequency of 1.4 V and a center frequency of 960 MHz was designed and simulated. The design has a gain of 28dB and a noise figure of 16 dB. The LNA has a real impedance of 47.9 Ohms. The $S_{11}$ and $S_{22}$ are –40 dB and –0417 dB respectively.

A CMOS mixer operating at a voltage of 3.3V having RF signal with frequency 960 MHz and an IF signal with frequency 950 MHz was designed and simulated.

This project made clear to us the various tradeoffs and sacrifices that have to be made when designing analog RF circuits to meet stringent specifications which is evident in our circuit.

REFERENCES


