ABSTRACT

Two circuits satisfying the functional requirements of a low noise amplifier and a mixer were designed and simulated using Agilent’s ADS2003A EDA tools. A 960 MHz single-ended LNA and a single-balanced active mixer were developed for a 0.5-micron CMOS process using the Level 3 model. The simulated gain of the amplifier was 20 dB with a noise figure of approximately 1.2 dB. The simulated gain of the mixer was 15 dB. A design procedure and the simulation results for both are presented in this report.
INTRODUCTION

A low noise amplifier is usually the first stage of a receiver coming off the antenna. In wireless communications systems, the signal detected by the antenna has very low power and the LNA must provide both good gain and good noise performance. The gain must be sufficiently high to overcome the noise of subsequent stages, and noise performance is of importance because the overall noise figure of a receiver is dominated by the first stages of the design.

A mixer converts a signal from a higher frequency ($\omega_{RF}$) to a lower one ($\omega_{IF}$); if active, it might also provide significant gain. A mixer receives the RF signal directly from the LNA, or from a filter—depending on the receiver architecture, and performs frequency translation by multiplying it with another signal provided by a local oscillator (LO). This multiplication yields two signals in the frequency spectrum at $\omega_{RF} \pm \omega_{IF}$. Linearity in a mixer design is of high importance to prevent intermodulations caused by interferers.

DESIGN PROCEDURE

The first step in the design process was to analyze the I-V characteristics of a CMOS transistor. Understanding biasing as well as the effects of varying the W/L ratio of a transistor was essential. Then, the high frequency analysis of a CMOS transistor equivalent-circuit was studied to comprehend the internal functionality of the transistor and the effects of its parasitic capacitances; particularly, the gate-to-source capacitance ($C_{GS}$) and its effects on circuit performance at high frequencies. Throughout the design process, the width value of the transistors for the circuit had to be chosen carefully to control $C_{GS}$.

LNA

After reviewing several common LNA architectures, the single-ended cascode architecture with source degeneration was selected. As reference, the schematic shown in Figure 1 was used [2]:

![Figure 1: Cascode LNA](image-url)
In a cascode configuration, the common-source input stage, represented by MOSFET 2 in Figure 1, achieves high input resistance and a large $g_m$, which is important for gain. Also, the common-gate stage (MOSFET 1) improves the high-frequency response of the amplifier, and its good for reverse isolation [1].

The LC circuit formed by L3 and C1 is used to tune the frequency response of the LNA, and to achieve better gain and noise figure.

SPECIFICATIONS

The following step was to create an LNA design that met the design requirements given. The specifications were the following:

- Frequency range: 940~980 MHz
- Input impedance $Z_{IN}$: $|Z_{IN}| = 50 \text{ ohm} \pm 10\%$, $<Z_{IN} = 0 \pm 2.5 \text{ degree}$
- Voltage gain: $A_v > 20 \text{ dB}$
- Noise Figure: NF with 50 ohm input matching $< 3 \text{ dB}$
- $P_{1dB} > -20 \text{ dBm}$
- $I_{IP3} > -10 \text{ dBm}$
- Total current $< 5 \text{ mA}$

FINAL DESIGN

According to [2], component values were calculated to build the schematic for an amplifier meeting the desired specs. The final schematic is shown in Figure 2:

![Figure 2: Final design – LNA](image-url)
A 2.5V source was used to power up the circuit. The DC biasing was established using transistor chains acting as voltage dividers. A 2nH inductor and a 12.24pF capacitor were used as the LC tuning circuit.

SIMULATION SETUP

To analyze the performance of the LNA design, it was necessary to learn and understand the different simulation types available in ADS (DC, AC, Harmonic Balance, S-Parameters, etc). After some investigation, an S-parameter simulation was chosen to measure the reflection voltage coefficients at the input and output terminals, the noise figure, the gain, and the input and output impedances. The actual setup consisted on adding DC blocking components to the input and output ports, and then terminating them with matching terminals of 50 and 1600 Ohm respectively.

Once the simulation environment was set up, simulations were performed. The results are provided in the simulation results section of this report.

MIXER

The architecture chosen for the mixer design was that of a single-balanced active mixer. The reasons for this were that the LNA design was single-ended, and also it was desired to achieve gain while downconverting the RF signal. As a reference, the schematic shown in Figure 3 was used [1]:

![Active Mixer Schematic](image)

**Figure 3: Active Mixer**

In the architecture shown in Figure 3, the RF input (V RF) varies the drain current of MOSFET 3, which is biased in the saturation region. The LO input causes MOSFETS 1 and 2 to act as a switching pair.

SPECIFICATIONS

The specifications followed for designing the mixer were the following:
• RF\text{\textit{input}}: V_{RF} = 0.001 \sin(2\pi f_{RF} t) V \ ; f_{RF} = 960 \text{ MHz}

• LO (positive node): V_{LO+} = 2+0.2 \sin(2\pi f_{LO} t) V \ ; f_{LO} = 940 \text{ MHz}

• LO (negative node): V_{LO-} = 2-0.2 \sin(2\pi f_{LO} t) V \ ; f_{LO} = 940 \text{ MHz}

• IF output = V_{IF}

FINAL DESIGN

Figure 4 shows the schematic for the final design:

A 3.3V source was used to power up the circuit. NMOS and PMOS transistors with very small width to length ratios to keep the noise figure low were used to set the DC bias. Also, for biasing purposes, an active current source was connected to the source terminal of MOSFET 1—the RF input transistor.

The \textit{W} chosen for MOSFET 1 was 900 \text{um}. This in combination with the current source formed by MOSFETS 9 and 3 generated a drain current of 0.5 mA for MOSFET 1, which was biased in the saturation operating region with \textit{V}_{GS} = 710 mV, \textit{V}_{TH} = 690 mV, and \textit{V}_{DS} = 1.16 V.

SIMULATION SETUP

To observe the behavior of our mixer, a 0.1mV, 960 MHz \textit{V_1 Tone} source was applied to the RF port of the mixer to simulate an RF input signal. The source and the mixer were coupled with a 100 \text{pF} capacitor. To control the switching pair of transistors, a differential LO signal was generated utilizing a 950 MHz
\(V_{1Tone}\) source passed through a transformer with a 1:1 turn ratio (arbitrarily chosen), and then delivering it to the gate terminals of the switching pair for control purposes. The type of simulation chosen to run the mixer in ADS was Harmonic Balance. A load resistance of 1.5 kOhm was used to drive the mixer.

The simulation results are provided in the next section.

**SIMULATION RESULTS**

**LNA**

A 50 \(\Omega\) input impedance was obtained by fine-tuning the value of \(L_2\), and adjusting the W/L ratio of MOSFET 1 to get the appropriate \(C_{GS}\) that, combined with \(L_2\), could set the imaginary part of the impedance to zero and set 960 MHz as the resonant frequency at the input. Z-parameter measurements were taken. Observe in Figure 5 that the real part of the input impedance is almost 50 \(\Omega\), while the imaginary part is almost cancelled.

![Figure 5: Z_{11} parameter - Input Impedance](image)

In Figure 6, it can be observed that the real and imaginary parts of the output impedance at 960 MHz have an approximate value of 1600 and 45 respectively. This indicates that for maximum power transfer, the LNA output must be terminated with a 1600 \(\Omega\) load.

![Figure 6: Z_{22} parameter - Output Impedance](image)
Originally, the amplification level desired from the LNA was a 20dB gain in a passband of 940 to 980 MHz. However, the final design satisfied the gain specification only for a passband of approximately 955 to 965 MHz. This is shown in the $S_{21}$ parameter graph provided in Figure 7. As expected, the gain curve peaks at the desired center frequency –960 MHz, but then it drops sharply to the sides, falling by almost 12 dB at 940 and 980 MHz.

Finally, the most important design specification was getting a noise figure of 3dB or less. As seen in Figure 8, the NF measured for this particular design is about 1.2dB and hence meets the design requirement. Also in Figure 8, it is shown that the total current drawn by the LNA was 4.96 mA.

<table>
<thead>
<tr>
<th>freq</th>
<th>Ii</th>
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<tbody>
<tr>
<td>0.0000 Hz</td>
<td>4.963 mA</td>
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DC Current drawn by LNA

Unfortunately, due to time constraints and lack of experience in working with ADS, several difficulties were encountered when trying to calculate $P_{1dB}$ and $IIP_3$; these measurements were not taken.

MIXER

A single-tone, 100 uV, 960 MHz signal was applied to the mixer as an RF input. The spectrum of the RF input is shown in Figure 9.
A single-tone, 20 mV, 950 MHz signal was used to generate the LO differential signal to control the switching pair of the mixer. Figure 10 shows the spectrum of the LO signal before passing through the transformer.

A Harmonic Balance simulation was performed to downconvert the RF signal to a lower frequency. Figure 11 shows the result. A significant component in the spectrum is observed at 950 MHz, implying severe LO leakage.
Figure 12 is a zoomed-in version of Figure 11. Here, special attention is given to the lower frequencies. It can be ratified that the downconversion process was performed correctly, since the presence of a component in the spectrum at 10 MHz is found. Moreover, a strong component at 0 Hz is also observed, which implies that the LO leakage introduced a DC offset.

From Figures 9 to 12, it can be estimated that the gain conversion for this circuit is approximately 15 dB, and the magnitude of the DC offset in dBs is –11 dB. The total current necessary for the mixer to operate is lower than 3 mA.

REFERENCES

