Modeling MOS Transistors

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Modeling MOSFETs for simulation

- Software is used to simulate circuits for validation
- Original program – SPICE – UC Berkeley
  - Simulation Program with Integrated Circuit Emphasis
- Other programs:
  - IBM’s internal ASX – developers work closely with Berkeley
  - Synopsys’ HSPICE (most commonly used?)
  - Cadence Spectre
  - Cadence PSPICE – used for PCB simulation (not really ICs)
  - Agilent’s ADS and Ansofts Nexxim (for RF simulation)
  - NGSPICE – at sourceforge.com for free
  - SPICE OPUS
MOSFET models

- Simulation models are
  - used in circuit simulators to simulate transistor behavior
  - created by device engineers
  - and used by circuit designers to validate larger designs

- Transistor models
  - take as input
    - voltages at four terminals (drain, source, gate, body)
    - environmental conditions (temperature, noise)
  - generate as output currents and capacitances

- Several levels of models:
  - Level 1 is based on GCA analysis in previous chapter
  - BSIM is latest and accounts for deep sub-micron effects
MOSFET models – Level 1

- Based on Gradual Channel Approximation
- Good for long channel devices
- low accuracy and slow
- Ignores deep sub-micron effects
- Ignores sub-threshold current (Ioff)
- Includes device parameters – physical and electrical:
  - VTO – no body bias threshold voltage
  - KP – transconductance
  - LAMBDA – channel modulation coefficient
  - PHI – surface inversion potential
  - GAMMA – body effect coefficient
  - and much more (30 or so more)
MOSFET models – level 1 device model

- Based on Gradual Channel Approximation
- Not accurate or fast
Correlating Model to cross section

- Field Oxide
- P+
- Field Oxide
- Source N+
- Drain N+
- Field Oxide
- Silicon Substrate
gate to body oxide capacitances
Capacitance between gate and substrate

\[ C_{gb} \]
source / drain oxide capacitances

- Based on Gradual Channel Approximation
- Not accurate or fast
Oxide capacitance is always present between gate and both source and drain although this cap tends to be small.

\[
C_{gs} = \frac{W \cdot L_d \cdot \varepsilon_{ox}}{t_{ox}}
\]
Oxide capacitance is split between $C_{gs}$ and $C_{gd}$ in linear mode. Substrate is shielded by inversion layer. Also includes small overlap capacitance.

\[
C_{gs} = C_{ds} = \frac{1}{2} \cdot \frac{W \cdot L \cdot \varepsilon_{ox}}{t_{ox}} + C_{ov}
\]
Oxide capacitance is to incomplete inversion layer which provides a connection to the source only. Gate to drain cap is limited to overlap only.

\[
C_{gs} = \frac{2}{3} \frac{W \cdot L \cdot \varepsilon_{ox}}{t_{ox}} + C_{ov}
\]
MOSFET models - junction capacitance

![MOSFET circuit diagram with capacitance labels: $C_{gd}$, $C_{gs}$, $C_{gb}$, $C_{db}$, $C_{sb}$, $V_{gs}$, $V_{ds}$, gate, drain, source, bulk.]
Oxide Capacitance – Saturation Mode

Junction capacitance increases with increases in doping and decreases with increases in reverse bias voltage.

SOI virtually eliminates this capacitance.
MOSFET models – series resistance

- \( C_{gd} \)
- \( C_{gs} \)
- \( C_{gb} \)
- \( C_{db} \)
- \( C_{sb} \)

- Gate
- Drain
- Source
- Bulk

\[ + V_{gs} - \]
\[ + V_{ds} - \]
As source / drain junction depth (Xj) decreases with each new technology generation, source drain series resistance is growing.
Simple SPICE program

*Spice Input File (deck) for an inverter
VIN in gnd PULSE(0 1.0 2ns 2ns 2ns 50ns 100ns)
* d g s b model
mp out in vdd vdd PMOS L=0.18u W=0.8u
mn out in gnd gnd NMOS L=0.18u W=0.4u

.tran 0.1ns 20ns 0n 100p
.print TRAN V(out) V(in)
.model P1 PMOS Level=1
  +VT0=0.35 KP=2.0e-5 GAMMA=0.37 PHI=0.65 LAMBDA=0.02
  +RD=1.0 RS=1.0
.model N1 NMOS Level=1
  +VT)=0.35 KP=4.0e-5 GAMMA=0.37 PHI=0.65 LAMBDA=0.02
  +RD=1.0 RS=1.0
.end
Simple SPICE program

*Spice Input File (deck) for a NAND gate
VIN in gnd PULSE(0 1.0 2ns 2ns 2ns 50ns 100ns)
*   d    g   s    b    model
mpa out a  vdd  vdd  PMOS L=0.18u  W=0.8u
mpa out b  vdd  vdd  PMOS L=0.18u  W=0.8u
mna out a  int  gnd  NMOS L=0.18u  W=0.8u
mna int b  gnd  gnd  NMOS L=0.18u  W=0.8u

.tran 0.1ns 20ns 0n 100p
.print TRAN V(out) V(a) V(b)
.include NMOS_MODEL
.include PMOS_MODEL
.end
MOSFET models – BSIM3

- Models generated by UC Berkeley
- Depends on empirical fitting
- includes Short Channel Effects (SCE)
  - Vt rolloff – Vts are influenced by Leffs at short channel length
  - mobilities
  - sub-threshold leakage
- Capacitance models the same but more accurate
- Source / Drain resistance
- Designed with computational speed in mind
- Used universally now
UFSOI models

- Models generated by University of Florida
- Incorporated into Berkeley Spice 3E5
- Models describe physical features of transistor
- Best models for SOI but can model bulk too.
- Used in this class
- Compiled for Sun machine, but we have source which could be ported to Linux or PC (extra credit?)
Specifying Source/Drain areas/perimeters

By specifying area and perimeters of the source and drain, the caps can be calculated for the area and sidewalls.

mp 0 1 2 2 PMOS L=0.18u W=5u AS=35p PS=24u AD=35p PD=24u
Spice in interactive mode
Spice in batch mode
Spice Example