Static (DC) Characteristics of MOS Inverters

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MOS Inverters

- Most fundamental circuit in MOS family
- Represents the basic operation of all static gates
- One input and one output
  - Output = ~Input
- Inverter Threshold Voltage - $V_{\text{th}}$
  - input voltage where output equals input
  - not the same as transistor threshold $V_t$
Voltage Transfer Characteristic (VTC) ideal

- Infinite gain at threshold
- Zero gain at all other input voltages
When Input high, NFET turns on and we have a voltage dividing resistor network consisting of the NFET (Low R) and Load (High R). Consequently, the output will be dropped down to $\frac{R_L}{R_L + R_H}$.

Current will be constant (bad) and equal to $\frac{V_{dd}}{R_L + R_H}$. 
When Input Low, NFET turns off and capacitor is charged fully to Vdd. No current runs through the load and no voltage drop exists across the load.
Voltage Transfer Characteristic (VTC)

- $V_{DD} = V_{OH}$
- $V_{TH}$
- $V_{IL}$
- $V_{IH}$

- $V_{out} = V_{in}$
- Gain = -1
Noise Margin – low gain region

\[ \text{gain} = -1 \]
Noise Margin – high gain region

Vout

Vin

High gain region

Gain = -1

Good design minimizes high gain region aka transition region.
Noise Margin

Vin

Vih

transition region indeterminate

Vil

Vout

Voh

NM_H = V_{oh} - V_{ih}

NM_L = V_{oL} - V_{iL}
Single Source Noise Margin

If $V_n$ is less than noise margin than the noise will be attenuated each stage and will quickly disappear.

If $V_n$ is greater than the noise margin, the noise will result in voltages at the input that will be in the high gain region and will be amplified through subsequent stages.
Resistive Load Inverter

\[ |I_{rl}| = I_{ds} \]

\[ \frac{V_{dd}}{R_L} \]

\[ V_{ol} \]

\[ V_{oh}=V_{dd} \]
Resistive Load Inverter – Voh and Vol

**Voh**

Voh = Vdd because when the input voltage drops below Vt of the inverter, no current flows. No current flow in turn means no voltage drop across the load resistor and Vout = Vdd = Voh.

**Vol**

If the input is driven to Voh=Vdd then the transistor is on and since Vgs > Vds it is also in linear mode. The drain will be at Vol and the gate will be at Voh.

\[
I_{ds} = I_r = \frac{1}{2} \cdot K \cdot \left[ 2 \cdot (V_{gs} - V_{t0}) \cdot V_{ds} - V_{ds}^2 \right] = \frac{V_{dd} - V_{ol}}{R}
\]

\[
V_{ol} \approx V_{dd} - V_t + \frac{1}{KR} - 1 + K \cdot R_l (V_{dd} - V_t)
\]
Resistive Load Inverter – Vil

\( \text{To determine noise margin we need } V_{il} \text{ which is one of two points where we have unity gain. When input low, output high and NFET in saturation.} \)

\[
I_{ds} = I_r = \frac{1}{2} \cdot K \cdot (V_{gs} - V_{t0})^2 = \frac{V_{dd} - V_{out}}{R}
\]

\[
V_{il} = V_t + \frac{1}{KR_l}
\]
Resistive Load Inverter – Vih

When Vin = Vih, the output is at Vol and the NFET is in the linear region.

\[ I_{ds} = I_r = \frac{1}{2} \cdot K \cdot \left[ 2 \cdot (V_{gs} - V_{t0}) \cdot V_{ds} - V_{ds}^2 \right] = \frac{V_{dd} - V_{ol}}{R} \]

\[ V_{ih} = V_{t+} \sqrt{\frac{8V_{dd}}{3kR}} - \frac{1}{kR_l} \]
Resistive Load Inverter – Vth

\[ I_{ds} = I_r = \frac{1}{2} \cdot K \cdot (V_{in} - V_{t0})^2 = \frac{V_{dd} - V_{out}}{R} \]

\[ V_{in} = V_{out} = V_{th} \]

\[ \frac{1}{2} \cdot K \cdot (V_{th} - V_{t0})^2 = \frac{V_{dd} - V_{th}}{R} \]

Solve for \( V_{th} \) in quadratic equation. Correct root should be between 0 and \( V_{dd} \).
Resistive Load Inverter – Static Power

\[ P = V \cdot I \]

\[ I_{ds} = I_r = \frac{V_{dd} - V_{out}}{R} \]

\[ P = (50\%) \cdot V_{dd} \cdot \frac{V_{dd} - V_{out}}{R} \]
Resistive Load Inverter VTC

Vin

Vout

kR=2V^{-1}

kR=4V^{-1}

kR=8V^{-1}
Enhancement NFET Load Inverter

$I_I = I_d$

Two power supplies needed to keep load conducting while $V_{out} = V_{dd}$.
Depletion NFET Load Inverter

Load NFET is always on and acts like a non-linear resistor.

Requires two types of NFETs.
Depletion NFET Load Inverter

\[ V_{oh} = V_{dd} \]

\[ V_{ol} \approx 0 \]

\[ V_{il} = V_{t0} + \left( \frac{K_l}{K_d} \right) \cdot \left[ V_{out} - V_{dd} + V_{tload}(V_{out}) \right] \]

Solve for \( V_{th} \) in quadratic equation.
Correct root should be between 0 and \( V_{dd} \)
CMOS Inverter

![CMOS Inverter Diagram](image)

Vout = Vin - Vtp

Vout = Vin - Vtn

Vout = Vtn

Vout = Vdd + Vtp

Vout = Vin - Vtp

Vout = Vin - Vtn
CMOS Inverter – Noise Margin

\[ V_{oh} = V_{dd} \]

\[ V_{ol} = gnd \]

\[ V_{ih} = \frac{V_{dd} + V_{to} + k_r \cdot (2 \cdot V_{out} + V_{tn})}{1 + k_r} \]

\[ V_{il} = \frac{2V_{out} + V_{tp} - V_{dd} + k_r \cdot V_{tn}}{1 + k_r} \]

\[ V_{tn} = \sqrt{\frac{1}{k_r} (V_{dd} + V_{tp})} \]

\[ V_{th} = \frac{1}{1 + \sqrt{\frac{1}{k_r}}} \]
Layout of inverter – top view
Layout of inverter – top view

- vdd
- gnd
- source
- gate
- drain
- input
- out
- in
- I1
- I2
CMOS Tri-state Inverter

Diagram showing a CMOS tri-state inverter with inputs labeled as 'input', 'en', and the output labeled as 'output'. The schematic includes transistors and logic gates.
CMOS Inverters - Summary

- At normal input levels, little static power
- What happens if input is floated?
- Dynamic Power only during transitions
- In transition region, short circuit current exists
- Very good noise properties
- Body effect is irrelevant as no stacked transistors
- Transconductance ratio determines $V_{th}$