Chip IO

Prof. MacDonald
IO as seen by logic designer
Goals of IO design

- Reduce delay to and from outside world (PCB)
- High drive current capability
- Match impedance to load
- ESD Protection
- Level shifting of voltages (i.e. 1.2V inside/3.3V outside)
- Meet specifications of Interfaces
- Reduce power (short circuit current through output buffers)
- High voltage tolerance
IO Cells and Placement

Wirebond IO
Interface signaling standards

- Single ended vs. Differential
- Levels – Voh, Vol, Vih, Vil
- Termination
- Most common Interfaces
  - TTL is old school – Transistor-Transistor Logic
    - term used generically for 5V single-ended logic
    - not really used for last 25 years
  - CMOS and LVCMOS
    - 5V, 3.3V, 2.5V, 1.8V, 1.5V and 1.2V (technology driven)
    - Vil ~ 0.8V,
    - Vih ~ 0.75*Vdd
Recent Interface Standards

- **SSTL (Stub Series Terminated Logic)**
  - Interface for commodity DRAM memory
  - Double pumped at rising / falling edge of clock
  - 200, 266, 300 MHz at 2.5V
  - Clock is differential – 2 opposite signals
  - Data is single ended - terminated to midpoint
    - High quiescent current

- **SDRAM DDR II**
  - Same as before with 1.8V and faster
Figure 33: Input Voltage Waveform

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NOTE:
1. VTH (MIN) with test load is 1.927V
2. Vol (MAX) with test load is 0.375V
3. For Non-DDR400 devices, numbers in diagram reflect nominal values utilizing circuit below.
Recent Interface Standards

- LVDS (Low Voltage Differential Signaling)
  - Used for really high speed operation (500MHz <)
    - Example: 200 MSPS 12bit ADC
  - Data is sent in pairs that run +/- 0.35 from midpoint
  - Differential mode improves noise sensitivity
    - noise affects both lines and is cancelled out
  - reduce voltage swing improves speed
  - reduce voltage swing improves dynamic power
    - but termination cause hugh static power
  - Base for many competing serial interconnects
New Serial Interconnects

- Gigabit speeds
- Similar to Ethernet, but broader use
- RapidIO
- Infiniband
- HyperTransport
- PCI-express
<table>
<thead>
<tr>
<th>Cell Name</th>
<th>Description</th>
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<tbody>
<tr>
<td>PCI33DGZ</td>
<td>3-STATE OUTPUT PCI BUFFER PAD WITH INPUT AND LIMITED SLEW RATE, 5V-Tolerant</td>
</tr>
<tr>
<td>PCI66DGZ</td>
<td>3-STATE OUTPUT PCI BUFFER PAD WITH INPUT AND LIMITED SLEW RATE, 5V-Tolerant</td>
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<tr>
<td>PDBxDGZ</td>
<td>CMOS 3-State Output Pad with Input, 5V-Tolerant</td>
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<tr>
<td>PDDDGZ</td>
<td>Input Pad With Pulldown, 5-VT IO</td>
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<tr>
<td>PDDSDGZ</td>
<td>Schmitt Trigger Input Pad, 5V-Tolerant</td>
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<tr>
<td>PDDxDGZ</td>
<td>CMOS 3-State Output Pad with Input and Pulldown, 5V-Tolerant</td>
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<td>PDIDGZ</td>
<td>Input Pad, 5V-Tolerant</td>
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<td>PDISDGZ</td>
<td>Schmitt Trigger Input Pad, 5V-Tolerant</td>
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<td>PDOxCDG</td>
<td>CMOS Output Pad</td>
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<tr>
<td>PDTxDGZ</td>
<td>CMOS 3-State Output Pad, 5V-Tolerant</td>
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<td>PDUDGZ</td>
<td>Input Pad With Pullup, 5V-Tolerant</td>
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<td>PDUSDGZ</td>
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<td>PDUxDGZ</td>
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<td>PDXOExDG</td>
<td>Crystal Oscillator with High Enable</td>
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<tr>
<td>PDOxCDG</td>
<td>Crystal Oscillator</td>
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<td>PRBxDGZ</td>
<td>CMOS 3-State Output Pad with Input and Limited Slew Rate, 5V-Tolerant</td>
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<td>PRDxDGZ</td>
<td>CMOS 3-State Output Pad with Input, Pulldown, and Limited Slew Rate, 5V-Tolerant</td>
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<tr>
<td>PROxCDG</td>
<td>CMOS Output Pad with Limited Slew Rate</td>
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<td>PVDDxDGZ</td>
<td>Vdd Pad</td>
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<tr>
<td>PVSSxDGZ</td>
<td>Vss Pad</td>
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IO Libraries - Artisan TSMC

Truth Table

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<tr>
<th>INPUT</th>
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Cell Information

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<tr>
<th>Cell Name</th>
<th>No. Pad Req.</th>
<th>Power (uW/MHz)</th>
<th>Drive Capability (mA)</th>
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Pin Capacitance (pF)

<table>
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<th>Cell Name</th>
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<th>OEN</th>
<th>PAD</th>
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</thead>
<tbody>
<tr>
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<td>0.046</td>
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<td>0.060</td>
<td>5.435</td>
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<tr>
<td>PDD04DGZ</td>
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<td>0.107</td>
<td>0.060</td>
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<td>PDD24DGZ</td>
<td>0.046</td>
<td>0.114</td>
<td>0.068</td>
<td>5.141</td>
</tr>
</tbody>
</table>

Propagation Delays (ns)
VDD, OVDD and GNDs

- Guidelines for VDD, OVDD, and GNDs
  - Need sufficient VDD and GNDs to avoid electromigration
  - Need sufficient OVDD and GNDs to avoid droop and bounce
    - Guideline is 6 outputs for each pair of OVDD and GND
  - Simultaneous switching - independent of freq.
Simultaneous Switching

- Consider a 64 bit output bus
- If all transition from high to low,
- lots of current must be sunk by gnd
- Voltage drop will develop from gndi and gnde
- Extent can be measured on quiet low output
- Problem is independent of frequency
- Causes compression of supply voltage and thus results in unexpected slow down.
Simultaneous Switching

- Identify SS IO and spread them out
- Avoid placing near asynch inputs
- Can use low slew IO - but performance suffers
- Stagger timing of outputs
- At most 6 outputs per power pin pair
- 3 outputs per power pin is rock solid
- Add decoupling caps between Ovdd and Gnd
- Decrease cap load on outputs
Design of basic CMOS IO

• **Output buffer must be very large**
  • needs to drive pF not fF – 1000’s time larger than normal
  • presents huge load to internal logic
    • so requires increasing fanout inverter chain to be driven
  • short circuit current is unacceptable
    • so pullup/pulldown must be mutually exclusive
Design of basic CMOS IO

- Output buffer may run at higher voltage
  - Internal Core is 1.95V max for 0.18u technology
  - However most other chips run at 3.3V

1.8V – not high enough to turn PFET off

GND is too low for PFET causes 3.3V drop across gate oxide
Input Buffers

- Input buffer drives internal logic
  - General much smaller than output buffer
  - May need to downshift signal voltage with 0Vt device
ESD protection

• Static discharge is like a grenade to dainty CMOS transistors
  • cause gate oxide to rupture
  • permanent damage to chips

• Three models
  • human body model (low energy – high voltage – 2kV typical)
  • machine body model (higher energy)
  • charge body model (another model – can’t remember)

• All CMOS chips are tested as a part of reliability studies to measure ESD levels that can be withstood.
ESD protection

- If bond pad exceeds Vdd + diode drop, top diode turns on and discharges static
- If bond pad drops below one diode drop below ground, bottom diode turns on
- In either case, the gate oxide of the input buffer is protected.
IO circuit with level shifters
Level Shifters

Fig. 20. Layout view of I/O driver.