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## Revision History

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<th>Revision Date</th>
<th>Effective Date</th>
<th>Author</th>
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<td>-</td>
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<td>06-06-2001</td>
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<td>Updated the description of ATDDIEN and PORTAD1 register.</td>
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<td>16-06-2001</td>
<td>-</td>
<td></td>
<td>Made SRS2 Compliant</td>
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<td>20 June 2001</td>
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<td>V02.07</td>
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<td>Corrected Table &quot;Available Result Data Formats&quot;</td>
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<td>V02.08</td>
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Section 1 Introduction

1.1 Overview

The ATD_10B8C is an 8-channel, 10-bit, multiplexed input successive approximation analog-to-digital converter. Refer to device electrical specifications for ATD accuracy.

The block is designed to be upwards compatible with the 68HC11 standard 8-bit A/D converter. In addition, there are new operating modes that are unique to the HC12 design.

1.2 Features

- 8/10 Bit Resolution.
- 7 µsec, 10-Bit Single Conversion Time.
- Sample Buffer Amplifier.
- Programmable Sample Time.
- Left/Right Justified, Signed/Unsigned Result Data.
- External Trigger Control.
- Conversion Completion Interrupt Generation.
- Analog Input Multiplexer for 8 Analog Input Channels.
- Analog/Digital Input Pin Multiplexing.
- 1 to 8 Conversion Sequence Lengths.
- Continuous Conversion Mode.
- Multiple Channel Scans.

1.3 Modes of Operation

1.3.1 Conversion modes

There is software programmable selection between performing single or continuous conversion on a single channel or multiple channels.

1.3.2 MCU Operating Modes

- Stop Mode
  Entering Stop Mode causes all clocks to halt and thus the system is placed in a minimum power standby mode. This aborts any conversion sequence in progress. During recovery from Stop Mode, there must be a minimum delay for the Stop Recovery Time tSR before initiating a new ATD conversion sequence.
**1.4 Block Diagram**

![ATD_10B8C Block Diagram](image)

Figure 1-1  ATD_10B8C Block Diagram

- **Wait Mode**
  Entering Wait Mode the ATD conversion either continues or aborts for low power depending on the logical value of the AWAIT bit.

- **Freeze Mode**
  In Freeze Mode the ATD_10B8C will behave according to the logical values of the FRZ1 and FRZ0 bits. This is useful for debugging and emulation.
Section 2  Signal Description

2.1 Overview

The ATD_10B8C has a total of 12 external pins.

2.2 Detailed Signal Descriptions

2.2.1  AN7 / ETRIG / PAD7

This pin serves as the analog input Channel 7. It can be configured to provide an external trigger for the ATD conversion. It can be configured as general purpose digital input.

2.2.2  AN6 / PAD6

This pin serves as the analog input Channel 6. It can be configured as general purpose digital input.

2.2.3  AN5 / PAD5

This pin serves as the analog input Channel 5. It can be configured as general purpose digital input.

2.2.4  AN4 / PAD4

This pin serves as the analog input Channel 4. It can be configured as general purpose digital input.

2.2.5  AN3 / PAD3

This pin serves as the analog input Channel 3. It can be configured as general purpose digital input.

2.2.6  AN2 / PAD2

This pin serves as the analog input Channel 2. It can be configured as general purpose digital input.

2.2.7  AN1 / PAD1

This pin serves as the analog input Channel 1. It can be configured as general purpose digital input.

2.2.8  AN0 / PAD0

This pin serves as the analog input Channel 0. It can be configured as general purpose digital input.
2.2.9 VRH, VRL

VRH is the high reference voltage and VRL is the low reference voltage for ATD conversion.

2.2.10 VDDA, VSSA

These pins are the power supplies for the analog circuitry of the ATD_10B8C block.
Section 3 Memory Map and Register Definition

3.1 Overview

This section provides a detailed description of all registers accessible in the ATD_10B8C.

3.2 Module Memory Map

Table 3-1 gives an overview on all ATD_10B8C registers.

<table>
<thead>
<tr>
<th>Address Offset</th>
<th>Use</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>$._00</td>
<td>ATD Control Register 0 (ATDCTL0)(^1)</td>
<td>R</td>
</tr>
<tr>
<td>$._01</td>
<td>ATD Control Register 1 (ATDCTL1)(^2)</td>
<td>R</td>
</tr>
<tr>
<td>$._02</td>
<td>ATD Control Register 2 (ATDCTL2)</td>
<td>R/W</td>
</tr>
<tr>
<td>$._03</td>
<td>ATD Control Register 3 (ATDCTL3)</td>
<td>R/W</td>
</tr>
<tr>
<td>$._04</td>
<td>ATD Control Register 4 (ATDCTL4)</td>
<td>R/W</td>
</tr>
<tr>
<td>$._05</td>
<td>ATD Control Register 5 (ATDCTL5)</td>
<td>R/W</td>
</tr>
<tr>
<td>$._06</td>
<td>ATD Status Register 0 (ATDSTAT0)</td>
<td>R/W</td>
</tr>
<tr>
<td>$._07</td>
<td>Unimplemented</td>
<td></td>
</tr>
<tr>
<td>$._08</td>
<td>ATD Test Register 0 (ATDTEST0)(^3)</td>
<td>R</td>
</tr>
<tr>
<td>$._09</td>
<td>ATD Test Register 1 (ATDTEST1)</td>
<td>R/W</td>
</tr>
<tr>
<td>$._0A</td>
<td>Unimplemented</td>
<td></td>
</tr>
<tr>
<td>$._0B</td>
<td>ATD Status Register 1 (ATDSTAT1)</td>
<td>R</td>
</tr>
<tr>
<td>$._0C</td>
<td>Unimplemented</td>
<td></td>
</tr>
<tr>
<td>$._0D</td>
<td>ATD Input Enable Register (ATDDIEN)</td>
<td>R/W</td>
</tr>
<tr>
<td>$._0E</td>
<td>Unimplemented</td>
<td></td>
</tr>
<tr>
<td>$._0F</td>
<td>Port Data Register (PORTAD)</td>
<td>R</td>
</tr>
<tr>
<td>$._10, $._11</td>
<td>ATD Result Register 0 (ATDDR0H, ATDDR0L)</td>
<td>R/W</td>
</tr>
<tr>
<td>$._12, $._13</td>
<td>ATD Result Register 1 (ATDDR1H, ATDDR1L)</td>
<td>R/W</td>
</tr>
<tr>
<td>$._14, $._15</td>
<td>ATD Result Register 2 (ATDDR2H, ATDDR2L)</td>
<td>R/W</td>
</tr>
<tr>
<td>$._16, $._17</td>
<td>ATD Result Register 3 (ATDDR3H, ATDDR3L)</td>
<td>R/W</td>
</tr>
<tr>
<td>$._18, $._19</td>
<td>ATD Result Register 4 (ATDDR4H, ATDDR4L)</td>
<td>R/W</td>
</tr>
<tr>
<td>$._1A, $._1B</td>
<td>ATD Result Register 5 (ATDDR5H, ATDDR5L)</td>
<td>R/W</td>
</tr>
<tr>
<td>$._1C, $._1D</td>
<td>ATD Result Register 6 (ATDDR6H, ATDDR6L)</td>
<td>R/W</td>
</tr>
<tr>
<td>$._1E, $._1F</td>
<td>ATD Result Register 7 (ATDDR7H, ATDDR7L)</td>
<td>R/W</td>
</tr>
</tbody>
</table>

NOTES:
1. ATDCTL0 is intended for factory test purposes only.
2. ATDCTL1 is intended for factory test purposes only.
3. ATDTEST0 is intended for factory test purposes only.

**NOTE:** Register Address = Base Address + Address Offset, where the Base Address is defined at the MCU level and the Address Offset is defined at the module level.
3.3 Register Descriptions

This section describes in address order all the ATD_10B8C registers and their individual bits.

3.3.1 Reserved Register (ATDCTL0)

This register is reserved for factory testing and is not available in normal modes.

Read: always read $00 in normal modes
Write: unimplemented in normal modes

NOTE: Writing to this registers when in special modes can alter functionality.

3.3.2 Reserved Register (ATDCTL1)

This register is reserved for factory testing and is not available in normal modes.

Read: always read $00 in normal modes
Write: unimplemented in normal modes

NOTE: Writing to this registers when in special modes can alter functionality.
3.3.3 ATD Control Register 2 (ATDCTL2)

This register controls power down, interrupt and external trigger. Writes to this register will abort current conversion sequence but will not start a new sequence.

![Figure 3-3 ATD Control Register 2 (ATDCTL2)](image)

Read: anytime
Write: anytime

ADPU — ATD Power Down
This bit provides on/off control over the ATD_10B8C block allowing reduced MCU power consumption. Because analog electronic is turned off when powered down, the ATD requires a recovery time period after ADPU bit is enabled.

1 = Normal ATD functionality
0 = Power down ATD

AFFC — ATD Fast Flag Clear All
1 = Changes all ATD conversion complete flags to a fast clear sequence. Any access to a result register will cause the associate CCF flag to clear automatically.
0 = ATD flag clearing operates normally (read the status register ATDSTAT1 before reading the result register to clear the associate CCF flag).

AWAI — ATD Power Down in Wait Mode
When entering Wait Mode this bit provides on/off control over the ATD_10B8C block allowing reduced MCU power. Because analog electronic is turned off when powered down, the ATD requires a recovery time period after exit from Wait mode.

1 = Power down ATD during Wait mode
0 = ATD continues to run in Wait mode

ETRIGE — External Trigger Level/Edge Control
This bit controls the sensitivity of the external trigger signal. See Table 3-2 for details.

ETRIGP — External Trigger Polarity
This bit controls the polarity of the external trigger signal. See Table 3-2 for details.
ETRIGE — External Trigger Mode Enable

This bit enables the external trigger on ATD channel 7. The external trigger allows to synchronize sample and ATD conversions processes with external events.

1 = Enable external trigger
0 = Disable external trigger

**NOTE:** The conversion results for the external trigger ATD channel 7 have no meaning while external trigger mode is enabled.

ASCIE — ATD Sequence Complete Interrupt Enable

1 = ATD Interrupt will be requested whenever ASCIF=1 is set.
0 = ATD Sequence Complete interrupt requests are disabled.

ASCIF — ATD Sequence Complete Interrupt Flag

If ASCIE=1 the ASCIF flag equals the SCF flag (see 3.3.7), else ASCIF reads zero. Writes have no effect.

1 = ATD sequence complete interrupt pending
0 = No ATD interrupt occurred

### 3.3.4 ATD Control Register 3 (ATDCTL3)

This register controls the conversion sequence length, FIFO for results registers and behavior in Freeze Mode. Writes to this register will abort current conversion sequence but will not start a new sequence.

<table>
<thead>
<tr>
<th>ETRIGE</th>
<th>ETRIGP</th>
<th>External Trigger Sensitivity</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>falling edge</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>rising edge</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>low level</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>high level</td>
</tr>
</tbody>
</table>

**Table 3-2 External Trigger Configurations**

**Figure 3-4 ATD Control Register 3 (ATDCTL3)**

Read: anytime
Write: anytime
S8C, S4C, S2C, S1C — Conversion Sequence Length

These bits control the number of conversions per sequence. Table 3-3 shows all combinations. At reset, S4C is set to 1 (sequence length is 4). This is to maintain software continuity to HC12 family.

Table 3-3 Conversion Sequence Length Coding.

<table>
<thead>
<tr>
<th>S8C</th>
<th>S4C</th>
<th>S2C</th>
<th>S1C</th>
<th>Number of Conversions per Sequence</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>8</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>2</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>3</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>4</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>5</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>6</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>8</td>
</tr>
</tbody>
</table>

FIFO — Result Register FIFO Mode

If this bit is zero (non-FIFO mode), the A/D conversion results map into the result registers based on the conversion sequence; the result of the first conversion appears in the first result register, the second result in the second result register, and so on.

If this bit is one (FIFO mode) the conversion counter is not reset at the beginning or end of a conversion sequence; conversion results are placed in consecutive result registers between sequences. The result register counter wraps around when it reaches the end of the result register file. The conversion counter value in ATDSTAT0 can be used to determine where in the result register file, the current conversion result will be placed.

Finally, which result registers hold valid data can be tracked using the conversion complete flags. Fast flag clear mode may or may not be useful in a particular application to track valid data.

1 = Conversion results are placed in consecutive result registers (wrap around at end).
0 = Conversion results are placed in the corresponding result register up to the selected sequence length.

FRZ1, FRZ0 — Background Debug Freeze Enable

When debugging an application, it is useful in many cases to have the ATD pause when a breakpoint (Freeze Mode) is encountered. These 2 bits determine how the ATD will respond to a breakpoint as shown in Table 3-4. Leakage onto the storage node and comparator reference capacitors may compromise the accuracy of an immediately frozen conversion depending on the length of the freeze period.

Table 3-4 ATD Behavior in Freeze Mode (breakpoint)

<table>
<thead>
<tr>
<th>FRZ1</th>
<th>FRZ0</th>
<th>Behavior in Freeze mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Continue conversion</td>
</tr>
</tbody>
</table>
3.3.5 ATD Control Register 4 (ATDCTL4)

This register selects the conversion clock frequency, the length of the second phase of the sample time and the resolution of the A/D conversion (i.e.: 8-bits or 10-bits). Writes to this register will abort current conversion sequence but will not start a new sequence.

**Table 3-4 ATD Behavior in Freeze Mode (breakpoint)**

<table>
<thead>
<tr>
<th>FRZ1</th>
<th>FRZ0</th>
<th>Behavior in Freeze mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>Reserved</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Finish current conversion, then freeze</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Freeze Immediately</td>
</tr>
</tbody>
</table>

Figure 3-5  ATD Control Register 4 (ATDCTL4)

Read: anytime

Write: anytime

SRES8 — A/D Resolution Select

This bit selects the resolution of A/D conversion results as either 8 or 10 bits. The A/D converter has an accuracy of 10 bits. However, if low resolution is required, the conversion can be speeded up by selecting 8-bit resolution.

1 = 8 bit resolution
0 = 10 bit resolution

SMP1, SMP0 — Sample Time Select

These two bits select the length of the second phase of the sample time in units of ATD conversion clock cycles. Note that the ATD conversion clock period is itself a function of the prescaler value (bits PRS4-0). The sample time consists of two phases. The first phase is two ATD conversion clock cycles long and transfers the sample quickly (via the buffer amplifier) onto the A/D machine’s storage node. The second phase attaches the external analog signal directly to the storage node for final charging and high accuracy. **Table 3-5** lists the lengths available for the second sample phase.

**Table 3-5 Sample Time Select**

<table>
<thead>
<tr>
<th>SMP1</th>
<th>SMP0</th>
<th>Length of 2nd phase of sample time</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>2 A/D conversion clock periods</td>
</tr>
</tbody>
</table>
These 5 bits are the binary value prescaler value PRS. The ATD conversion clock frequency is calculated as follows:

\[
\text{ATDclock} = \frac{[\text{BusClock}]}{[\text{PRS} + 1]} \times 0.5
\]

Note that the maximum ATD conversion clock frequency is half the Bus Clock. The default (after reset) prescaler value is 5 which results in a default ATD conversion clock frequency that is Bus Clock divided by 12. Table 3-6 illustrates the divide-by operation and the appropriate range of the Bus Clock.

### Table 3-6 Clock Prescaler Values

<table>
<thead>
<tr>
<th>Prescale Value</th>
<th>Total Divisor Value</th>
<th>Max. Bus Clock(^1)</th>
<th>Min. Bus Clock(^2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>00000</td>
<td>divide by 2</td>
<td>4 MHz</td>
<td>1 MHz</td>
</tr>
<tr>
<td>00001</td>
<td>divide by 4</td>
<td>8 MHz</td>
<td>2 MHz</td>
</tr>
<tr>
<td>00010</td>
<td>divide by 6</td>
<td>12 MHz</td>
<td>3 MHz</td>
</tr>
<tr>
<td>00011</td>
<td>divide by 8</td>
<td>16 MHz</td>
<td>4 MHz</td>
</tr>
<tr>
<td>00100</td>
<td>divide by 10</td>
<td>20 MHz</td>
<td>5 MHz</td>
</tr>
<tr>
<td>00101</td>
<td>divide by 12</td>
<td>24 MHz</td>
<td>6 MHz</td>
</tr>
<tr>
<td>00110</td>
<td>divide by 14</td>
<td>28 MHz</td>
<td>7 MHz</td>
</tr>
<tr>
<td>00111</td>
<td>divide by 16</td>
<td>32 MHz</td>
<td>8 MHz</td>
</tr>
<tr>
<td>01000</td>
<td>divide by 18</td>
<td>36 MHz</td>
<td>9 MHz</td>
</tr>
<tr>
<td>01001</td>
<td>divide by 20</td>
<td>40 MHz</td>
<td>10 MHz</td>
</tr>
<tr>
<td>01010</td>
<td>divide by 22</td>
<td>44 MHz</td>
<td>11 MHz</td>
</tr>
<tr>
<td>01011</td>
<td>divide by 24</td>
<td>48 MHz</td>
<td>12 MHz</td>
</tr>
<tr>
<td>01100</td>
<td>divide by 26</td>
<td>52 MHz</td>
<td>13 MHz</td>
</tr>
<tr>
<td>01101</td>
<td>divide by 28</td>
<td>56 MHz</td>
<td>14 MHz</td>
</tr>
<tr>
<td>01110</td>
<td>divide by 30</td>
<td>60 MHz</td>
<td>15 MHz</td>
</tr>
<tr>
<td>01111</td>
<td>divide by 32</td>
<td>64 MHz</td>
<td>16 MHz</td>
</tr>
<tr>
<td>10000</td>
<td>divide by 34</td>
<td>68 MHz</td>
<td>17 MHz</td>
</tr>
<tr>
<td>10001</td>
<td>divide by 36</td>
<td>72 MHz</td>
<td>18 MHz</td>
</tr>
<tr>
<td>10010</td>
<td>divide by 38</td>
<td>76 MHz</td>
<td>19 MHz</td>
</tr>
<tr>
<td>10011</td>
<td>divide by 40</td>
<td>80 MHz</td>
<td>20 MHz</td>
</tr>
<tr>
<td>10100</td>
<td>divide by 42</td>
<td>84 MHz</td>
<td>21 MHz</td>
</tr>
<tr>
<td>10101</td>
<td>divide by 44</td>
<td>88 MHz</td>
<td>22 MHz</td>
</tr>
<tr>
<td>10110</td>
<td>divide by 46</td>
<td>92 MHz</td>
<td>23 MHz</td>
</tr>
<tr>
<td>10111</td>
<td>divide by 48</td>
<td>96 MHz</td>
<td>24 MHz</td>
</tr>
<tr>
<td>11000</td>
<td>divide by 50</td>
<td>100 MHz</td>
<td>25 MHz</td>
</tr>
<tr>
<td>11001</td>
<td>divide by 52</td>
<td>104 MHz</td>
<td>26 MHz</td>
</tr>
<tr>
<td>11010</td>
<td>divide by 54</td>
<td>108 MHz</td>
<td>27 MHz</td>
</tr>
<tr>
<td>11011</td>
<td>divide by 56</td>
<td>112 MHz</td>
<td>28 MHz</td>
</tr>
<tr>
<td>11100</td>
<td>divide by 58</td>
<td>116 MHz</td>
<td>29 MHz</td>
</tr>
<tr>
<td>11101</td>
<td>divide by 60</td>
<td>120 MHz</td>
<td>30 MHz</td>
</tr>
<tr>
<td>11110</td>
<td>divide by 62</td>
<td>124 MHz</td>
<td>31 MHz</td>
</tr>
<tr>
<td>11111</td>
<td>divide by 64</td>
<td>128 MHz</td>
<td>32 MHz</td>
</tr>
</tbody>
</table>
NOTE:

1. Maximum ATD conversion clock frequency is 2MHz. The maximum allowed Bus Clock frequency is shown in this column.
2. Minimum ATD conversion clock frequency is 500KHz. The minimum allowed Bus Clock frequency is shown in this column.

3.3.6 ATD Control Register 5 (ATDCTL5)

This register selects the type of conversion sequence and the analog input channels sampled. Writes to this register will abort current conversion sequence and start a new conversion sequence.

Table 3-7 summarizes the result data formats available and how they are set up using the control bits.

Table 3-8 illustrates the difference between the signed and unsigned, left justified output codes for an input signal range between 0 and 5.12 Volts.
SCAN — Continuous Conversion Sequence Mode

This bit selects whether conversion sequences are performed continuously or only once.

1 = Continuous conversion sequences (scan mode)
0 = Single conversion sequence

MULT — Multi-Channel Sample Mode

When MULT is 0, the ATD sequence controller samples only from the specified analog input channel for an entire conversion sequence. The analog channel is selected by channel selection code (control bits CC/CB/CA located in ATDCTL5). When MULT is 1, the ATD sequence controller samples across channels. The number of channels sampled is determined by the sequence length value (S8C, S4C, S2C, S1C). The first analog channel examined is determined by channel selection code (CC, CB, CA control bits); subsequent channels sampled in the sequence are determined by incrementing the channel selection code.

1 = Sample across several channels.
0 = Sample only one channel.

CC, CB, CA — Analog Input Channel Select Code

These bits select the analog input channel(s) whose signals are sampled and converted to digital codes. Table 3-9 lists the coding used to select the various analog input channels. In the case of single channel scans (MULT=0), this selection code specified the channel examined. In the case of...
multi-channel scans (MULT=1), this selection code represents the first channel to be examined in the conversion sequence. Subsequent channels are determined by incrementing channel selection code; selection codes that reach the maximum value wrap around to the minimum value.

### Table 3-9 Analog Input Channel Select Coding

<table>
<thead>
<tr>
<th>CC</th>
<th>CB</th>
<th>CA</th>
<th>Analog Input Channel</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>AN0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>AN1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>AN2</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>AN3</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>AN4</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>AN5</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>AN6</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>AN7</td>
</tr>
</tbody>
</table>

#### 3.3.7 ATD Status Register 0 (ATDSTAT0)

This read-only register contains the Sequence Complete Flag, overrun flags for external trigger and FIFO mode, and the conversion counter.

<table>
<thead>
<tr>
<th>R/W</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>SCF</td>
<td>ETORF</td>
<td>FIFO</td>
<td>0</td>
<td>CC2</td>
<td>CC1</td>
<td>CC0</td>
<td></td>
</tr>
</tbody>
</table>

**Figure 3-7 ATD Status Register 0 (ATDSTAT0)**

Read: anytime

Write: anytime (No effect on (CC2, CC1, CC0))

**SCF — Sequence Complete Flag**

This flag is set upon completion of a conversion sequence. If conversion sequences are continuously performed (SCAN=1), the flag is set after each one is completed. This flag is cleared when one of the following occurs:
A) Write “1” to SCF
B) Write to ATDCTL5 (a new conversion sequence is started)
C) If AFFC=1 and read of a result register
   1 = Conversion sequence has completed
0 = Conversion sequence not completed

ETORF — External Trigger Overrun Flag
While in edge trigger mode (ETRIGLE=0), if additional active edges are detected while a conversion sequence is in process the overrun flag is set. This flag is cleared when one of the following occurs:
A) Write “1” to ETORF
B) Write to ATDCTL2, ATDCTL3 or ATDCTL4 (a conversion sequence is aborted)
C) Write to ATDCTL5 (a new conversion sequence is started)
   1 = External trigger over run error has occurred
   0 = No External trigger over run error has occurred

FIFOR - FIFO Over Run Flag.
This bit indicates that a result register has been written to before its associated conversion complete flag (CCF) has been cleared. This flag is most useful when using the FIFO mode because the flag potentially indicates that result registers are out of sync with the input channels. However, it is also practical for non-FIFO modes, and indicates that a result register has been over written before it has been read (i.e. the old data has been lost). This flag is cleared when one of the following occurs:
A) Write “1” to FIFOR
B) Start a new conversion sequence (write to ATDCTL5 or external trigger)
   1 = An over run condition exists
   0 = No over run has occurred

CC2, CC1, CC0 — Conversion Counter
These 3 read-only bits are the binary value of the conversion counter. The conversion counter points to the result register that will receive the result of the current conversion. E.g. CC2=1, CC1=1, CC0=0 indicates that the result of the current conversion will be in ATD Result Register 6. If in non-FIFO mode (FIFO=0) the conversion counter is initialized to zero at the begin and end of the conversion sequence. If in FIFO mode (FIFO=1) the register counter is not initialized. The conversion counters wraps around when its maximum value is reached.

3.3.8 Reserved Register (ATDTEST0)
This register is reserved for factory testing and is not available in normal modes.

<table>
<thead>
<tr>
<th>R</th>
<th>W</th>
<th>RESET:</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>6</td>
<td>5</td>
</tr>
</tbody>
</table>

Read: always read $00 in normal modes
Write: unimplemented in normal modes

**NOTE:** Writing to this register when in special modes can alter functionality.

### 3.3.9 ATD Test Register 1 (ATDTEST1)

This register contains the SC bit used to enable special channel conversions.

<table>
<thead>
<tr>
<th>R</th>
<th>W</th>
<th>RESET:</th>
<th>SC</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

![Figure 3-9 ATD Test Register 1 (ATDTEST1)](chart)

Read: anytime

Write: anytime

**SC - Special Channel Conversion Bit**

If this bit is set, then special channel conversion can be selected using CC, CB and CA of ATDCTL5. **Table 3-10** lists the coding.

- 1 = Special channel conversions enabled
- 0 = Special channel conversions disabled

**NOTE:** Always write remaining bits of ATDTEST1 (Bit7 to Bit1) zero when writing SC bit. Not doing so might result in unpredictable ATD behavior. Read of ATDTEST1 returns unpredictable values on Bit7 to Bit1.

### Table 3-10 Special Channel Select Coding

<table>
<thead>
<tr>
<th>SC</th>
<th>CC</th>
<th>CB</th>
<th>CA</th>
<th>Analog Input Channel</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>X</td>
<td>X</td>
<td>Reserved</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>$V_{RH}$</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>$V_{RL}$</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>$(V_{RH}+V_{RL})/2$</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
3.3.10 ATD Status Register 1 (ATDSTAT1)

This read-only register contains the Conversion Complete Flags.

Read: anytime  
Write: anytime, no effect

CCFx — Conversion Complete Flag x (x=7,6,5,4,3,2,1,0)

A conversion complete flag is set at the end of each conversion in a conversion sequence. The flags are associated with the conversion position in a sequence (and also the result register number). Therefore, CCF0 is set when the first conversion in a sequence is complete and the result is available in result register ATDDR0; CCF1 is set when the second conversion in a sequence is complete and the result is available in ATDDR1, and so forth. A flag CCFx (x=7,6,5,4,3,2,1,0) is cleared when one of the following occurs:
A) Write to ATDCTL5 (a new conversion sequence is started)  
B) If AFFC=0 and read of ATDSTAT1 followed by read of result register ATDDRx  
C) If AFFC=1 and read of result register ATDDRx

1 = Conversion number x has completed, result ready in ATDDRx  
0 = Conversion number x not completed

3.3.11 ATD Input Enable Register (ATDDIEN)

Read: anytime  
Write: anytime

IENx — Input Enable Flag x (x=7,6,5,4,3,2,1,0)

An input enable flag is set whenever the corresponding input channel is enabled for conversion. The flags are associated with the channel number. Therefore, IEN0 is set when channel 0 is enabled for conversion, IEN1 is set when channel 1 is enabled for conversion, and so forth. The flags are cleared when one of the following occurs:
A) Write to ATDCTL5 (a new conversion sequence is started)  
B) Write to ATDITR (a new conversion is initiated)  
C) If AFFC=1 and read of result register ATDDRx

1 = Input channel x enabled for conversion  
0 = Input channel x not enabled for conversion
IENx — ATD Digital Input Enable on channel x (x = 7, 6, 5, 4, 3, 2, 1, 0)

This bit controls the digital input buffer from the analog input pin (ANx) to PTADx data register.
1 = Enable digital input buffer to PTADx.
0 = Disable digital input buffer to PTADx

**NOTE:** Setting this bit will enable the corresponding digital input buffer continuously. If this bit is set while simultaneously using it as an analog port, there is potentially increased power consumption because the digital input buffer maybe in the linear region.

### 3.3.12 Port Data Register (PORTAD)

The data port associated with the ATD is input-only. The port pins are shared with the analog A/D inputs AN7-0.

<table>
<thead>
<tr>
<th>$0F$</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>PTAD7</td>
<td>PTAD6</td>
<td>PTAD5</td>
<td>PTAD4</td>
<td>PTAD3</td>
<td>PTAD2</td>
<td>PTAD1</td>
<td>PTAD0</td>
</tr>
<tr>
<td>W</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>RESET: AN7</td>
<td>AN6</td>
<td>AN5</td>
<td>AN4</td>
<td>AN3</td>
<td>AN2</td>
<td>AN1</td>
<td>AN0</td>
<td></td>
</tr>
</tbody>
</table>

= Unimplemented or Reserved

**Figure 3-12 Port Data Register (PORTAD)**

Read: anytime
Write: anytime, no effect

The A/D input channels may be used for general purpose digital input.

PTADx — A/D Channel x (ANx) Digital Input (x = 7, 6, 5, 4, 3, 2, 1, 0)

- If the digital input buffer on the ANx pin is enabled (IENx=1) read returns the logic level on ANx pin (signal potentials not meeting VIL or VIH specifications will have an indeterminate value).
- If the digital input buffers are disabled (IENx=0), read returns a “1”.
- Reset sets all PORTAD bits to “1”.

### 3.3.13 ATD Conversion Result Registers (ATDDRx)

The A/D conversion results are stored in 8 read-only result registers. The result data is formatted in the result registers based on two criteria. First there is left and right justification; this selection is made using the DJM control bit in ATDCTL5. Second there is signed and unsigned data; this selection is made using the DSGN control bit in ATDCTL5. Signed data is stored in 2’s complement format and only exists in left justified format. Signed data selected for right justified format is ignored.
Read: anytime  
Write: anytime, no effect

### 3.3.13.1 Left Justified Result Data

\[ \$._{10} = \text{ATDDR0H}, \$._{12} = \text{ATDDR1H}, \$._{14} = \text{ATDDR2H}, \$._{16} = \text{ATDDR3H} \]
\[ \$._{18} = \text{ATDDR4H}, \$._{1A} = \text{ATDDR5H}, \$._{1C} = \text{ATDDR6H}, \$._{1E} = \text{ATDDR7H} \]

<table>
<thead>
<tr>
<th>Bit</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>U</td>
<td>U</td>
<td>U</td>
<td>U</td>
<td>U</td>
<td>U</td>
<td>U</td>
<td></td>
</tr>
<tr>
<td>W</td>
<td>U</td>
<td>U</td>
<td>U</td>
<td>U</td>
<td>U</td>
<td>U</td>
<td>U</td>
<td></td>
</tr>
</tbody>
</table>

RESET: U U U U U U U 10-bit data

Figure 3-13 Left Justified, ATD Conversion Result Register, High Byte (ATDDRxH)

\[ \$._{11} = \text{ATDDR0L}, \$._{13} = \text{ATDDR1L}, \$._{15} = \text{ATDDR2L}, \$._{17} = \text{ATDDR3L} \]
\[ \$._{19} = \text{ATDDR4L}, \$._{1B} = \text{ATDDR5L}, \$._{1D} = \text{ATDDR6L}, \$._{1F} = \text{ATDDR7L} \]

<table>
<thead>
<tr>
<th>Bit</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>U</td>
<td>U</td>
<td>U</td>
<td>U</td>
<td>U</td>
<td>U</td>
<td>U</td>
<td></td>
</tr>
<tr>
<td>W</td>
<td>U</td>
<td>U</td>
<td>U</td>
<td>U</td>
<td>U</td>
<td>U</td>
<td>U</td>
<td></td>
</tr>
</tbody>
</table>

RESET: U U U U U U U 10-bit data

Figure 3-14 Left Justified, ATD Conversion Result Register, Low Byte (ATDDRxL)

### 3.3.13.2 Right Justified Result Data

\[ \$._{10} = \text{ATDDR0H}, \$._{12} = \text{ATDDR1H}, \$._{14} = \text{ATDDR2H}, \$._{16} = \text{ATDDR3H} \]
\[ \$._{18} = \text{ATDDR4H}, \$._{1A} = \text{ATDDR5H}, \$._{1C} = \text{ATDDR6H}, \$._{1E} = \text{ATDDR7H} \]

<table>
<thead>
<tr>
<th>Bit</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>U</td>
<td>U</td>
<td>U</td>
<td>U</td>
<td>U</td>
<td>U</td>
<td>U</td>
<td></td>
</tr>
<tr>
<td>W</td>
<td>U</td>
<td>U</td>
<td>U</td>
<td>U</td>
<td>U</td>
<td>U</td>
<td>U</td>
<td></td>
</tr>
</tbody>
</table>

RESET: U U U U U U U 10-bit data

Figure 3-15 Right Justified, ATD Conversion Result Register, High Byte (ATDDRxH)
Figure 3-16  Right Justified, ATD Conversion Result Register, Low Byte (ATDDRxL)

\[ \_11 = ATDDR0L, \_13 = ATDDR1L, \_15 = ATDDR2L, \_17 = ATDDR3L \]
\[ \_19 = ATDDR4L, \_1B = ATDDR5L, \_1D = ATDDR6L, \_1F = ATDDR7L \]

<table>
<thead>
<tr>
<th>R</th>
<th>BIT 7 MSB</th>
<th>BIT 7</th>
<th>BIT 6</th>
<th>BIT 5</th>
<th>BIT 4</th>
<th>BIT 3</th>
<th>BIT 2</th>
<th>BIT 1</th>
<th>BIT 0</th>
<th>10-bit data</th>
</tr>
</thead>
<tbody>
<tr>
<td>W</td>
<td>BIT 7 MSB</td>
<td>BIT 6</td>
<td>BIT 5</td>
<td>BIT 4</td>
<td>BIT 3</td>
<td>BIT 2</td>
<td>BIT 1</td>
<td>BIT 0</td>
<td></td>
<td>8-bit data</td>
</tr>
</tbody>
</table>

RESET: At reset the data format is left justified!

= Unimplemented or Reserved
Section 4  Functional Description

4.1 General

The ATD_10B8C is structured in an analog and a digital sub-block.

4.2 Analog Sub-block

The analog sub-block contains all analog electronics required to perform a single conversion. Separate power supplies VDDA and VSSA allow to isolate noise of other MCU circuitry from the analog sub-block.

4.2.1 Sample and Hold Machine

The Sample and Hold (S/H) Machine accepts analog signals from the external surroundings and stores them as capacitor charge on a storage node.

The sample process uses a two stage approach. During the first stage, the sample amplifier is used to quickly charge the storage node. The second stage connects the input directly to the storage node to complete the sample for high accuracy.

When not sampling, the sample and hold machine disables its own clocks. The analog electronics still draw their quiescent current. The power down (ADPU) bit must be set to disable both the digital clocks and the analog power consumption.

The input analog signals are unipolar and must fall within the potential range of VSSA to VDDA.

4.2.2 Analog Input Multiplexer

The analog input multiplexer connects one of the 8 external analog input channels to the sample and hold machine.

4.2.3 Sample Buffer Amplifier

The sample amplifier is used to buffer the input analog signal so that the storage node can be quickly charged to the sample potential.

4.2.4 Analog-to-Digital (A/D) Machine

The A/D Machine performs analog to digital conversions. The resolution is program selectable at either 8 or 10 bits. The A/D machine uses a successive approximation architecture. It functions by comparing the stored analog sample potential with a series of digitally generated analog potentials. By following a binary search algorithm, the A/D machine locates the approximating potential that is nearest to the sampled potential.
When not converting the A/D machine disables its own clocks. The analog electronics still draws quiescent current. The power down (ADPU) bit must be set to disable both the digital clocks and the analog power consumption.

Only analog input signals within the potential range of \( V_{RL} \) to \( V_{RH} \) (A/D reference potentials) will result in a non-railed digital output codes.

### 4.3 Digital Sub-block

This subsection explains some of the digital features in more detail. See register descriptions for all details.

#### 4.3.1 External Trigger Input (ETRIG)

The external trigger feature allows the user to synchronize ATD conversions to the external environment events rather than relying on software to signal the ATD module when ATD conversions are to take place. The input signal (ATD channel 7) is programmable to be edge or level sensitive with polarity control. Table 4-1 gives a brief description of the different combinations of control bits and their affect on the external trigger function.

<table>
<thead>
<tr>
<th>ETRIGLE</th>
<th>ETRIGP</th>
<th>ETRIGE</th>
<th>SCAN</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
<td>0</td>
<td>0</td>
<td>Ignores external trigger. Performs one conversion sequence and stops.</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>0</td>
<td>1</td>
<td>Ignores external trigger. Performs continuous conversion sequences.</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>X</td>
<td>Falling edge triggered. Performs one conversion sequence per trigger.</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>X</td>
<td>Rising edge triggered. Performs one conversion sequence per trigger.</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>X</td>
<td>Trigger active low. Performs continuous conversions while trigger is active.</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>X</td>
<td>Trigger active high. Performs continuous conversions while trigger is active.</td>
</tr>
</tbody>
</table>

During a conversion, if additional active edges are detected the overrun error flag ETORF is set.

In either level or edge triggered modes, the first conversion begins when the trigger is received. In both cases, the maximum latency time is one Bus Clock cycle plus any skew or delay introduced by the trigger circuitry.

**NOTE:** The conversion results for the external trigger ATD channel 7 have no meaning while external trigger mode is enabled.
Once ETRIGE is enabled, conversions cannot be started by a write to ATDCTL5, but rather must be triggered externally.

If the level mode is active and the external trigger both de-asserts and re-asserts itself during a conversion sequence, this does not constitute an overrun. Therefore, the flag is not set. If the trigger is left asserted in level mode while a sequence is completing, another sequence will be triggered immediately.

### 4.3.2 General Purpose Digital Input Port Operation

The input channel pins can be multiplexed between analog and digital data. As analog inputs, they are multiplexed and sampled to supply signals to the A/D converter. As digital inputs, they supply external input data that can be accessed through the digital port register PORTAD (input-only).

The analog/digital multiplex operation is performed in the input pads. The input pad is always connected to the analog inputs of the ATD_10B8C. The input pad signal is buffered to the digital port registers. This buffer can be turned on or off with the ATDDIEN register. This is important so that the buffer does not draw excess current when analog potentials are presented at its input.

### 4.3.3 Low Power Modes

The ATD_10B8C can be configured for lower MCU power consumption in 3 different ways:

- Stop Mode
- Wait Mode with AWAI=1
- Power down by writing ADPU=0 (Note that all ATD registers remain accessible.)

Note that the reset value for the ADPU bit is zero. Therefore, when this module is reset, it is reset into the power down state. Once the ATD_10B8C is configured for low power, it aborts any conversion sequence in progress. When ATD_10B8C powers up again (exit Stop Mode, exit Wait Mode with AWAI=1 or set ADPU=1), it requires a recovery time period.
Section 5  Resets

5.1 General

At reset the ATD_10B8C is in a power down state. The reset state of each individual bit is listed within the Register Description section (see Section 3 Memory Map and Register Definition) which details the registers and their bit-fields.
Section 6  Interrupts

6.1 General

The interrupt requested by the ATD_10B8C is listed in Table 6-1. Refer to MCU specification for related vector address and priority.

<table>
<thead>
<tr>
<th>Interrupt Source</th>
<th>CCR Mask</th>
<th>Local Enable</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sequence Complete Interrupt</td>
<td>I bit</td>
<td>ASCIE in ATDCTL2</td>
</tr>
</tbody>
</table>

See register descriptions for further details.