Computer Aided Digital Design

EE 3109
Fall 2009

Instructor: Ameet Chavan

Details
- Background/Prerequisites
  - EE2369 & EE2351
  - Knowledge of EE2369
- Office Hours - E309
- Website
- Textbook & Class notes

Course Outcomes
- Design combinational logic by using schematic capture tools and verify the circuit by simulation.
- Design sequential logic by using schematic capture tools and verify the circuit by simulation.
- Design complex digital circuits based on hierarchy approaches.
- Model and verify combinational logic by using VHDL language.
- Model and verify sequential logic by using VHDL language.
- Demonstrate competence in written technical communication.

Topics to be covered
- Basic capabilities and features of QUATRUS II. (1 hrs)
- Design and simulation of combinational logic. (2 hrs)
- Hierarchy design approach. (1 hr)
- Design and simulation of sequential logic. (3 hrs)
- Introduction to VHDL. (2 hrs)
- Design and simulation of combinational logic using VHDL. (2 hr)
- Design and simulation of sequential logic and state machine using VHDL. (3 hrs)

Reports
- Each report must include the following sections
  - Abstract
  - Introduction
  - Theory
  - Data & Analysis
  - Conclusions