Due: October 26, 2007

The purpose of this exercise is to become familiar with the VHDL language by implementing a 4-to-1 multiplexer. Use ALTERA QUATRUS II logic design tools for simulation.

I. Implement and verify a 4-to-1 multiplexer using ALTERA QUATRUS II. The following signals must included:
   a) D3, D2, D1, D0 as your inputs
   b) S1 and S0 as your control signals (also your inputs)
   c) Z as your output
   d) An ENABLE input signal to enable/disable the multiplexer.

II. Your report should contain the following
   a) The entire VHDL Code.
   b) Waveforms:
      1. For simplification use the following fixed values for your inputs:
         D3 = 1, D2 = 0, D1 = 1, D0 = 0. The waveform should show all the possible combinations for S1 and S0. The ENABLE signal must be zero in the middle.

III. Turn in the report before 5:00PM on the due date. Remember to write your report in the format that was given to you during the first class.

Reading:
   2. Class Notes