4-bit Adder/Subtracter

EE 3109 Computer Aided Digital Design - Lab Assignment #1

Pre-lab Due: September 12, 2007
Lab Due: September 14, 2007

The purpose of this exercise is to implement a 4-bit full adder/subtracter using a 1-bit full adder. This lab is divided into 2 parts. Use ALTERA QUATRUS II package to implement your circuit.

Part (a):

I. Implement and verify a 1-bit full adder using ALTERA QUATRUS II.
   The following are the steps needed:
   1. Use the QUATRUS II graphic editor to enter your logic circuit diagram.
   2. Compile the schematic produced in step 1.
   3. Construct a timing waveform for simulation. The waveform must include all the possible combinations.
      (End time – 40ns, Period – 10ns)
   4. Verify your logic design from step 2 by using the timing waveform constructed in step 3. This is when you actually simulate your circuit.
   5. Create a symbol for the schematic designed in step 1. This should be done after you verify the simulation waveforms in step 4.

II. Inputs and outputs
   1. Three inputs A, B and Cin.
   2. Two outputs Sum and Cout.

III. Your report must include the following

Part (b):

I. To implement the 4-bit adder/subtracter you need to use the symbol created in part (a). This should be done as follows:
   a. Use 4 of these symbols and other logic gates to design a 4-bit adder/subtracter that adds/subtracts binary numbers.
   b. Use signal ‘Add’ to control the addition/subtraction. Design it such that if “Add = 1” the circuit should add where as when “Add = 0” the circuit should subtract.

II. Inputs and outputs
   a. A3-A0, B3-B0 and Add (there should be a total of nine inputs; A3 & B3 are MSB’s).
   b. S4-S0 as outputs (there should be a total of 5 outputs; S4 is the MSB).

III. Operation:
   a. If “Add = 1”, the circuit should perform addition. For ex:- S4 S3 S2 S1 S0 = A3 A2 A1 A0 + B3 B2 B1 B0
   b. If “Add = 0”, the circuit should perform subtraction. For ex:- S4 S3 S2 S1 S0 = A3 A2 A1 A0 - B3 B2 B1 B0

IV. Your report must include the following
   a. Schematic Diagram
   b. Timing Waveform - Test your circuit with ATLEAST the following operations: (End time – 10ns)
      1. 0101 + 0011 (Add = 1) 2. 0110 – 0011 (Add = 0)

Reading:
   2. Class Notes